CLAIMS

What Is Claimed Is:

1. A method of using synchronous dynamic random access memory (SDRAM) to transmit data, the method comprising:

writing data using a first even addressed SDRAM bank;

writing data using a second even addressed SDRAM bank, wherein the first even addressed SDRAM bank and the second even addressed SDRAM bank write in parallel;

writing data using a first odd addressed SDRAM bank, wherein the first odd addressed SDRAM bank and the first even addressed SDRAM bank write interleaved; and

writing data using a second odd addressed SDRAM bank, wherein the second odd addressed SDRAM bank and the first odd addressed SDRAM bank write in parallel, and wherein the second odd addressed SDRAM bank and the second even addressed SDRAM bank write interleaved.

2. The method of Claim 1, wherein odd addressed SDRAM banks write interleaved with even addressed SDRAM banks.

3. The method of Claim 1, further comprising:

reading data using the first even addressed SDRAM bank;

reading data using the first odd addressed SDRAM bank, wherein the first even addressed SDRAM bank and the first odd addressed SDRAM bank read in parallel;

reading data using the second even addressed SDRAM bank, wherein the second even addressed SDRAM bank and the first even addressed SDRAM bank read interleaved; and

reading using the second odd addressed SDRAM bank, wherein the second odd addressed SDRAM bank and the second even addressed SDRAM bank read in parallel, and wherein the second odd addressed SDRAM bank and the first odd addressed SDRAM bank read interleaved.

4. The method of Claim 3, wherein even addressed SDRAM banks read interleaved with even addressed SDRAM banks, and wherein odd addressed SDRAM banks read interleaved with odd addressed SDRAM banks.

5. The method of Claim 1, further comprising:

determining whether a selection pointer is even or odd; and

selecting for a next operation either an odd addressed SDRAM bank or an even addressed SDRAM bank based on whether the selection pointer is even or odd.

6. The method of Claim 1, wherein one writing operation takes between 5 and 8 clock cycles to complete.

7. The method of Claim 3, wherein an amount of write operations is variable according to system requirements, and wherein an amount of read operations is variable according to system requirements.

8. The method of Claim 1, wherein the first even addressed SDRAM bank and the second even addressed SDRAM bank share a common data bus, and wherein the first odd addressed SDRAM bank and the second odd addressed SDRAM bank share a common data bus.

9. A method of transmitting data using synchronous dynamic random access memory (SDRAM), the method comprising:

writing data using a first set of SDRAM banks; and

writing data using a second set of SDRAM banks, wherein the first set of SDRAM banks and the second set of SDRAM banks write interleaved.

10. The method of Claim 9, further comprising:

reading data using a third set of SDRAM banks; and

reading data using a fourth set of SDRAM banks, wherein the fourth set of SDRAM banks and the third set of SDRAM banks read interleaved.

11. The method of Claim 9, wherein each set of SDRAM banks includes at least two SDRAM banks.

12. The method of Claim 10, wherein the first set of SDRAM banks and the third set of SDRAM banks share a common SDRAM bank.

13. An apparatus for transmitting data using synchronous dynamic random access memory (SDRAM), the apparatus comprising:

a first even addressed SDRAM bank;

a second even addressed SDRAM bank, wherein the first even addressed SDRAM bank and the second even addressed SDRAM bank are configured to write in parallel;

a first odd addressed SDRAM bank, wherein the first add addressed SDRAM bank and the first even addressed SDRAM bank are configured to write interleaved; and

a second odd addressed SDRAM bank, wherein the second odd addressed SDRAM bank and the first odd addressed

SDRAM bank are configured to write in parallel, and wherein the second odd addressed SDRAM bank and the second even addressed SDRAM bank are configured to write interleaved.

14. The apparatus of Claim 13, wherein each SDRAM bank is configured to read data, and wherein the first even addressed SDRAM bank and the first odd addressed SDRAM bank are configured to read in parallel, and wherein the second even addressed SDRAM bank and the first even addressed SDRAM bank are configured to read interleaved, and wherein the second odd addressed SDRAM bank and the second even addressed SDRAM bank are configured to read in parallel, and the second odd addressed SDRAM and the first odd addressed SDRAM bank are configured to read interleaved.

15. A computer-readable medium carrying one or more sequences of one or more instructions for transmitting data using synchronous dynamic random access memory (SDRAM), the one or more sequences of one or more instructions including instructions which, when executed by one or more processors, cause the one or more processors to perform the steps of:

writing data using a first even addressed SDRAM bank;

writing data using a second even addressed SDRAM bank, wherein the first even addressed SDRAM bank and the second even addressed SDRAM bank write in parallel;

writing data using a first odd addressed SDRAM bank, wherein the first odd addressed SDRAM bank and the first even addressed SDRAM bank write interleaved; and

writing data using a second odd addressed SDRAM bank, wherein the second odd addressed SDRAM bank and the first odd addressed SDRAM bank write in parallel, and wherein the second odd addressed SDRAM bank and the second even addressed SDRAM bank write interleaved.

16. The computer-readable medium of Claim 15, wherein odd addressed SDRAM banks write interleaved with even addressed SDRAM banks.

17. The computer-readable medium of Claim 15, wherein the instructions further cause the processor to carry out the steps of:

reading data using the first even addressed SDRAM bank;

reading data using the first odd addressed SDRAM bank, wherein the first even addressed SDRAM bank and the first odd addressed SDRAM bank read in parallel;

reading data using the second even addressed SDRAM bank, wherein the second even addressed SDRAM bank and the first even addressed SDRAM bank read interleaved; and

reading using the second odd addressed SDRAM bank, wherein the second odd addressed SDRAM bank and the second even addressed SDRAM bank read in parallel, and wherein the second odd addressed SDRAM bank and the first odd addressed SDRAM bank read interleaved.

18. The computer-readable medium of Claim 17, wherein even addressed SDRAM banks read interleaved with even addressed SDRAM banks, and wherein odd addressed SDRAM banks read interleaved with odd addressed SDRAM banks.

19. The computer-readable medium of Claim 15, wherein the instructions further cause the processor to carry out the steps of:

determining whether a selection pointer is even or odd; and

selecting for a next operation either an odd addressed SDRAM bank or an even addressed SDRAM bank based on whether the selection pointer is even or odd.

20. The computer-readable medium of Claim 15, wherein one writing operation takes between 5 and 8 clock cycles to complete.

21. The computer-readable medium of Claim 15, wherein an amount of write operations is variable according to system requirements, and wherein an amount of read operations is variable according to system requirements.

22. The computer-readable medium of Claim 15, wherein the first even addressed SDRAM bank and the second even addressed SDRAM bank share a common data bus, and wherein the first odd addressed SDRAM bank and the second odd addressed SDRAM bank share a common data bus.